CSE 206 (Digital Logic Design Sessional)

Experiment No.: 04

Name of the Experiment:

**Comparator, Adder/Sub tractor**

|  |  |
| --- | --- |
| Group No.: | 06 |
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| Section: | B2 |
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| Date of Performance: | 31/03/2021 |
| Date of Submission: | 03/04/2021 |

**Problem No. 01**

**Problem Specification:**

Design using basic gates, a 2-bit comparator to compare 2-bit numbers P and Q. The circuit should provide 3 output lines to indicate P>Q, P=Q and P<Q.

**Required Instruments:**

|  |  |  |  |
| --- | --- | --- | --- |
| **No** | **Name** | **Model** | **Quantity** |
| 01 | Logisim Software |  |  |
| 02 | IC(Hex-Inverter) | 74LS04 | 02 |
| 03 | IC (Quad 2 input AND) | 74LS08 | 02 |
| 04 | IC (Quad 2 input OR) | 74LS32 | 02 |
| 05 | IC (Quad 2 input XOR) | 74LS86 | 01 |
| 06 | Input Pins |  | 04 |
| 07 | Output Pins |  | 03 |
| 08 | Wires |  |  |

**Truth Table:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **P1** | **P0** | **Q1** | **Q0** | **A(P>Q)** | **B(P=Q)** | **C(P<Q)** |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 |

**Required Equations:**

**K-map for A (P>Q):**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Q1Q0  P1P0 | 00 | 01 | 11 | 10 |
| 00 | 0 | 0 | 0 | 0 |
| 01 | 1 | 0 | 0 | 0 |
| 11 | 1 | 1 | 0 | 1 |
| 10 | 1 | 1 | 0 | 0 |

A = f (P>Q)

= P0Q1’Q0’+ P1P0Q0’ + P1Q1’

= P1Q1’ + P0Q0’(Q1’+P1)

**K-map for B (P=Q):**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Q1Q0  P1P0 | 00 | 01 | 11 | 10 |
| 00 | 1 | 0 | 0 | 0 |
| 01 | 0 | 1 | 0 | 0 |
| 11 | 0 | 0 | 1 | 0 |
| 10 | 0 | 0 | 0 | 1 |

B = f (P = Q)

= P1P0Q1Q0 + P1’P0’Q1’Q0’ + P1’P0Q1’Q0 + P1P0’Q1Q0’

= P1’Q1’ (P0’Q0’+P0Q0) +P1Q1 (P0’Q0’+P0Q0)

= (P0’Q0’+P0Q0) (P1’Q1’+P1Q1)

= (P0⨁ Q0)’ (P1⨁ Q1)’

**K-map for C (P<Q):**

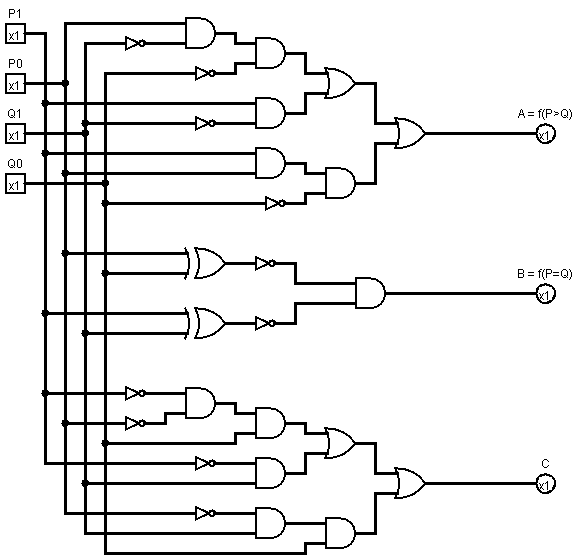
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Q1Q0  P1P0 | 00 | 01 | 11 | 10 |
| 00 | 0 | 1 | 1 | 1 |
| 01 | 0 | 0 | 1 | 1 |
| 11 | 0 | 0 | 0 | 0 |
| 10 | 0 | 0 | 1 | 0 |

C = f (P<Q)

= P1’P0’Q0 + P1’Q1 + P0’Q1Q0

= P0’Q0 (P1’+Q1) + P1’Q1

**Circuit Diagram:**



**Observation:**

1) We made a truth table and found out the output equations. We simplified the output equations and implemented the simplified form in our diagram.

2) We tried to make the circuit such a way that it was not too dense with wires

3) We used the documentations of the ICs to make sure the connections were given through the right pins.

4) We checked the output according to the truth table.

5) We can also take the NOR of (P>Q) and (P<Q) to implement the expression for (P=Q)

**Problem No. 02**

**Problem Specification:**

Design a 1-bit full sub tractor circuit using basic logic gates. Inputs are D, E and F denoting minuend, subtrahend and previous borrow respectively. The outputs are R and B representing the difference and output borrow.

**Required Instruments:**

|  |  |  |  |
| --- | --- | --- | --- |
| **No** | **Name** | **Model** | **Quantity** |
| 01 | Logisim Software |  |  |
| 02 | IC(Hex-Inverter) | 74LS04 | 01 |
| 03 | IC (Quad 2 input AND) | 74LS08 | 01 |
| 04 | IC (Quad 2 input OR) | 74LS32 | 01 |
| 05 | IC (Quad 2 input XOR) | 74LS86 | 01 |
| 06 | Input Pins |  | 03 |
| 07 | Output Pins |  | 02 |
| 08 | Wires |  |  |

**Truth Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **D** | **E** | **F** | **R** | **B** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**K-map for R:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| EF  D | 00 | 01 | 11 | 10 |
| 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |

R = D’E’F + D’EF’ + DE’F’ + DEF

= D’(E’F+EF’) + D(E’F’+EF)

= D ⊕ (E ⊕ F)

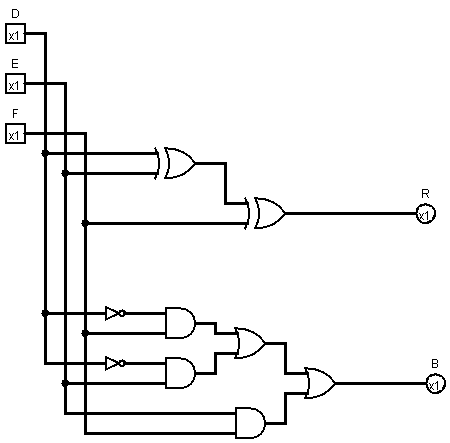
= D ⊕ E ⊕ F

**K-map for B:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| EF  D | 00 | 01 | 11 | 10 |
| 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 |

B = D’F + D’E + EF

**Circuit Diagram:**



**Observation:**

1) We made a truth table and found out the output equations. We simplified the output equations and implemented the simplified form in our diagram.

2) We tried to make the circuit such a way that it was not too dense with wires

3) We used the documentations of the ICs to make sure the connections were given through the right pins.

4) We checked the output according to the truth table.

5) We use the K-map method to simplify the circuit equations rather than Boolean algebra which is more precise and comprehensive

6) We have implemented a full sub tractor which can also be implemented with two half-sub tractor circuits.